

GS66508B-EVBDB GaN E-HEMT Daughter Board and GS665MB-EVB Evaluation Platform

User's Guide

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DANGER!

This evaluation kit is designed for engineering evaluation in a controlled lab environment and **should be handled by qualified personnel ONLY**. High voltage will be exposed on the board during the test and even brief contact during operation may result in severe injury or death.

Never leave the board operating unattended. After it is de-energized, always wait until all capacitors are discharged before touching the board.



CAUTION:

This product contains parts that are susceptible to damage by electrostatic discharge (ESD). Always follow ESD prevention procedures when handling the product.

Overview

The GS665XXX-EVBDB daughter board style evaluation kit consists of two GaN Systems 650V GaN Enhancement-mode HEMTs (E-HEMTs) and all necessary circuits including half bridge gate drivers, isolated power supplies and optional heatsink to form a functional half bridge power stage. It allows users to easily evaluate the GaN E-HEMT performance in any half bridge-based topology, either with the universal mother board (P/N: GS665MB-EVB) or users' own system design.

Features:

- Serves as a reference design and evaluation tool as well as deployment-ready solution for easy in-system evaluation.
- Vertical mount style with height of 35mm, which fits in majority of 1U design and allows evaluation of GaN E-HEMT in traditional through-hole type power supply board.
- Current shunt position for switching characterization testing
- Universal form factor and footprint for all products

The daughter board and universal mother board ordering part numbers are below:

Table 1 Ordering part numbers

Part Number	GaN E-HEMT P/N:	Description
GS66502B-EVBDB	GS66502B	GaN E-HEMT 650V/7.5A, 200mΩ
GS66504B-EVBDB	GS66504B	GaN E-HEMT 650V/15A, 100mΩ
GS66508B-EVBDB	GS66508B	GaN E-HEMT 650V/30A, 50mΩ
GS66508T-EVBDB	GS66508T	GaN E-HEMT top side cooled 650V/30A, 50mΩ
GS66516T-EVBDB	GS66516T	GaN E-HEMT top side cooled 650V/60A, 25mΩ
GS665MB-EVB		Universal 650V Mother Board

Control and Power I/Os:

The daughter board GS665XXX-EVBDB circuit diagram is shown in Figure 1. The control logic inputs on 2x3 pin header J1 are listed below:

Table 2 Control pins

Pin	Description
ENA	Enable input. It is internally pulled up to VCC, a low logic disables all the PWM gate drive outputs.
VCC	+5V auxiliary power supply input for logic circuit and gate driver. On the daughter board there are 2 isolated 5V to 9V DC/DC power supplies for top and bottom switches.
VDRV	Optional 9V gate drive power input. This pin allows users to supply separate gate drive power supply. By default VDRV is connected to VCC on the daughter board via a 0 ohm jumper FB1. If bootstrap mode is used for high side gate drive, connect VDRV to 9V
PWMH	High side PWM logic input for top switch Q1. It is compatible with 3.3V and 5V
PWML	Low side PWM logic input for bottom switch Q2. It is compatible with 3.3V and 5V
0V	Logic inputs and gate drive power supply ground return.

The 3 power pins are:

- VDC+: Input DC Bus voltage
- VSW: Switching node output
- VDC-: Input DC bus voltage ground return. Note that control ground 0V is isolated from VDC-.

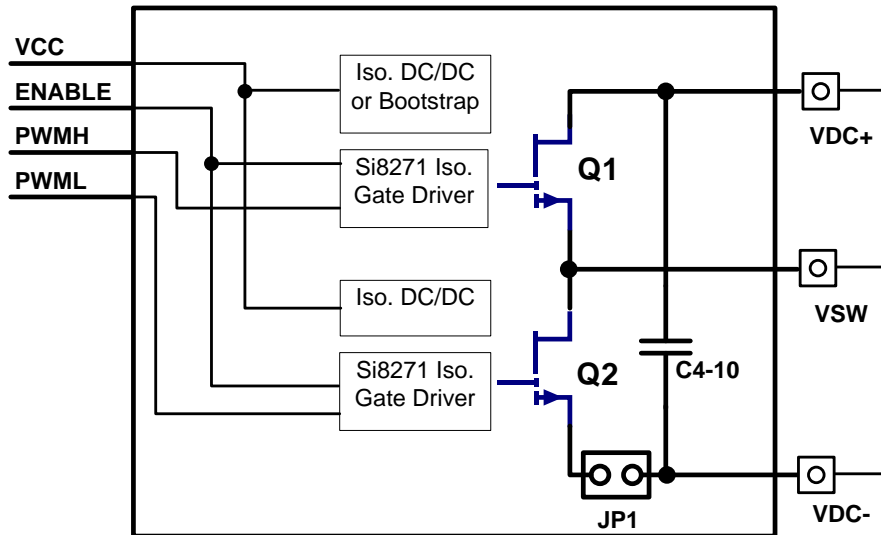


Figure 1 GS665XXX-EVBDB Evaluation Board Block Diagram

GS66508B-EVBDB half bridge daughter board

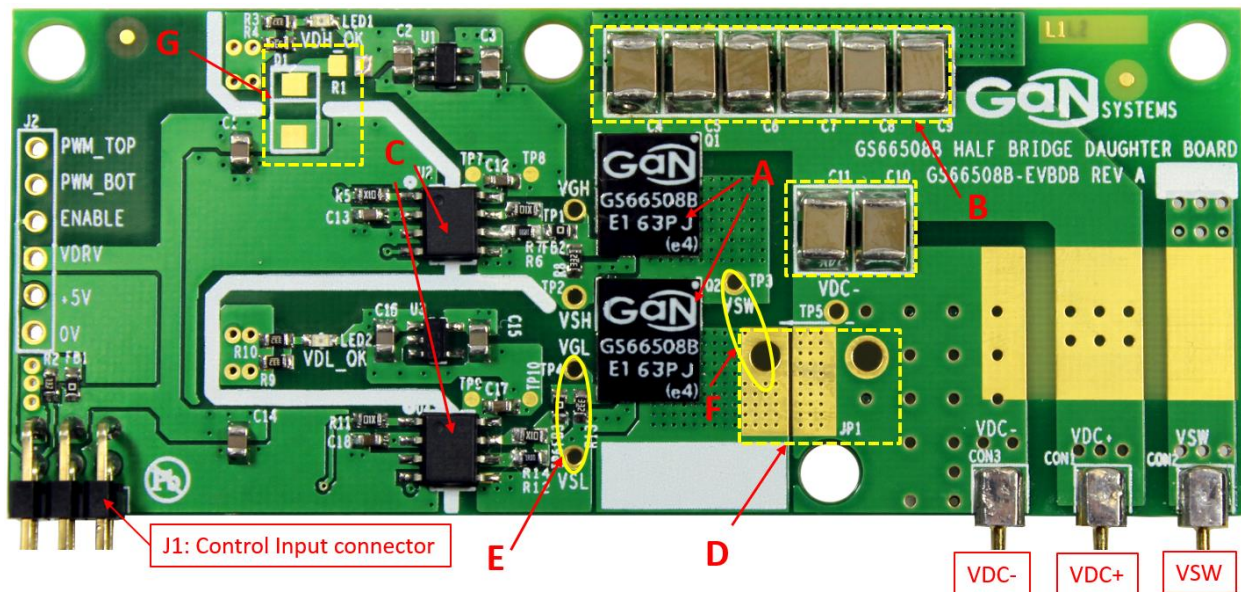


Figure 2 GS66508B-EVBDB top side

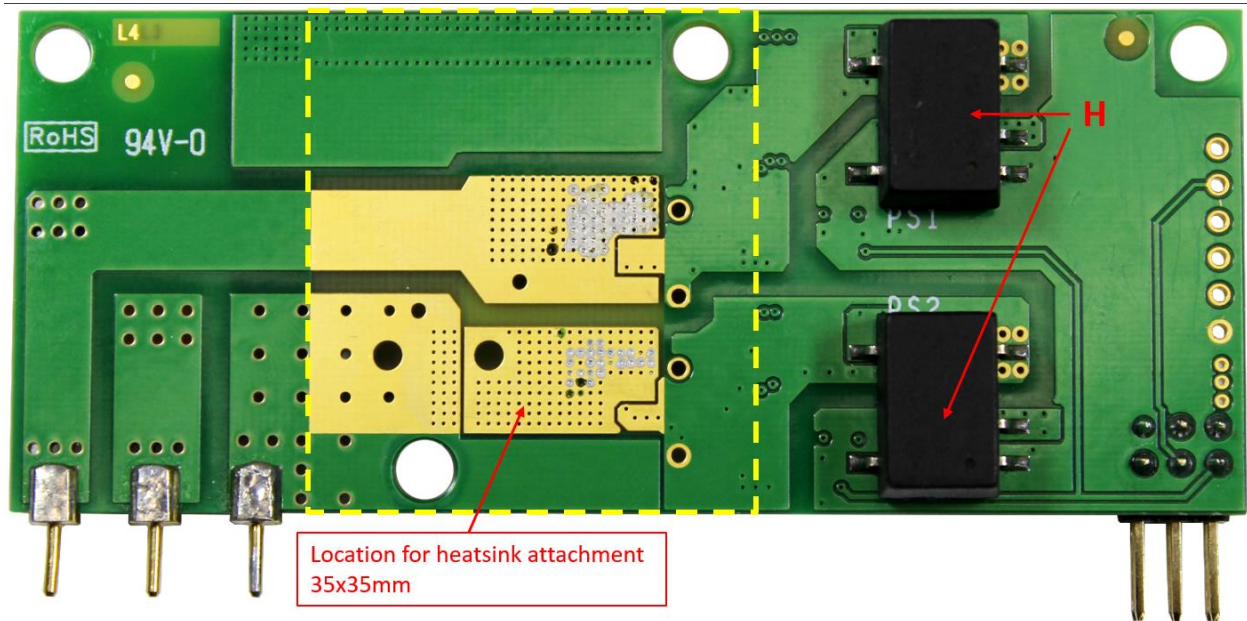


Figure 3 GS66508B-EVBDB bottom side

- A. 2x GaN Systems 650V E-HEMT GS66508B, 30A/50mΩ
- B. Decoupling capacitors C4-C11
- C. Isolated gate driver Silab Si8271GB-IS
- D. Optional current shunt position JP1.
- E. Test points for bottom Q2 V_{GS} .
- F. Recommended probing positions for Q2 V_{DS} .
- G. Optional bootstrap circuit D1/R1 (unpopulated).
- H. 5V-9V isolated DC/DC gate drive power supply

GaN E-HEMTs:

- This daughter board includes two GaN Systems E-HEMT GS66508B (650V/30A, 50mΩ) in a GaNPx™ B type package. The large S pad serves as source connection and thermal pad. The pin 4 is the kelvin source connection for gate drive return.

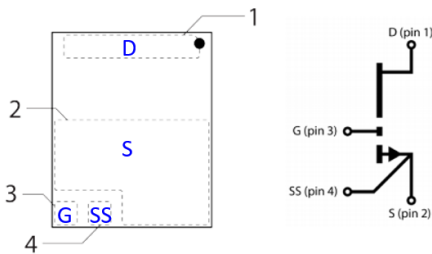


Figure 4 Package outline of GS66508B

Gate driver circuit:

- Silab Si8271GB-IS isolated gate driver is chosen for this design. This driver is compatible with 6V gate drive with 4V UVLO and has CMTI dv/dt rating up to 200V/ns. It has separated source and sink drive outputs which eliminates the need for additional diode.
- GaN E-HEMT switching speed and slew rate can be directly controlled by the gate resistor. By default the turn-on R_{gate} (R6/R12) is 10Ω and R_{g_off} (R7/R14) is 1Ω. User can adjust the values of gate resistors to fine tune the turn-on and off speed.
- FB1/FB2 are footprints for optional ferrite bead. By default they are populated with 0Ω jumpers. If gate oscillation is observed, it is recommended to replace them with ferrite bead with Z=10-20Ω@100MHz.

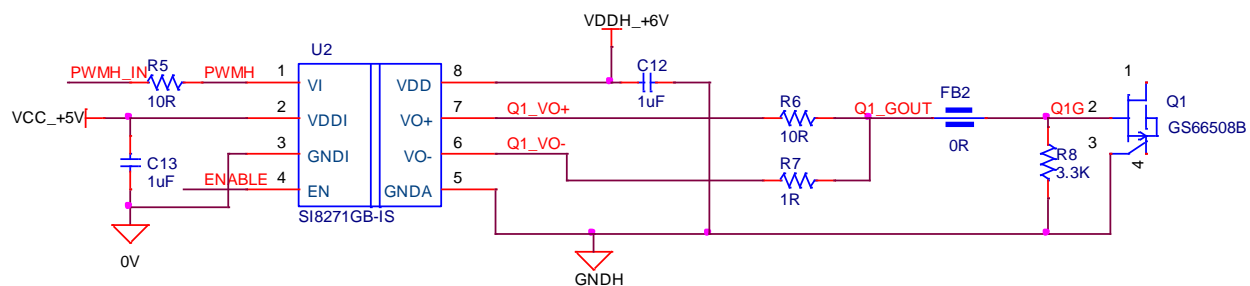


Figure 5 Gate driver circuit

Gate drive power supply:

- 5V-9V isolated DC/DC converters are used for gate drive. 9V output is then regulated down to 6V for gate driver.
- By default gate drive supply input VDRV is tied to VCC +5V via 0Ω jumper (FB1). Remove FB1 if separate gate drive input voltage is to be used.

Bootstrap mode:

- The board has option for users to experiment with non-isolated bootstrap circuit with following circuit changes:
 - Remove PS2 and short circuit pin 2 to 5 and pin 1 to 4.
 - Populate D1/ R1 (not supplied): D1 is the high voltage bootstrap diode (for example ES1J) and use 1-2Ω 0805 SMD resistor on R1. Depopulate PS1, LED1 and replace C2 with 1μF capacitor.
 - Remove 0Ω jumper at FB1 and supply +9V at VDRV.

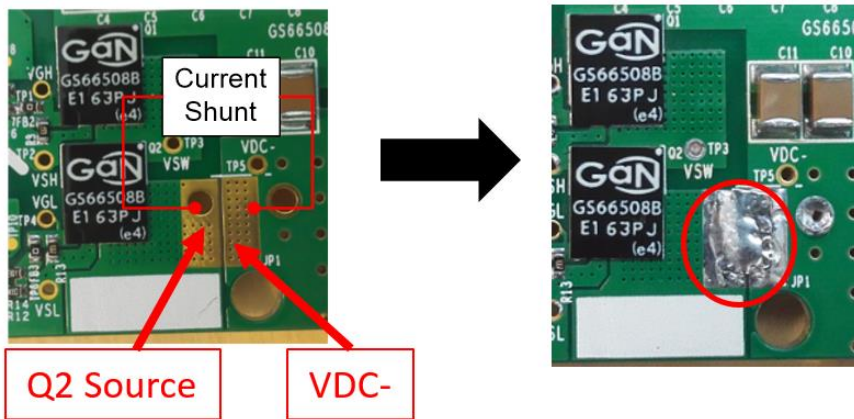


Figure 7 Current shunt position JP1

Measurement with current shunt:

1. When measuring VSW with current shunt, ensure all channel probe grounds and current shunt BNC output case are all referenced to the source end of Q2 before the current shunt. The recommended setup of probes is shown as below.
2. The output of coaxial current shunt can be connected to oscilloscope via 50Ω termination impedance to reduce the ringing.
3. The measured current is inverted and can be scaled by using: $I_d = V_{id} / R_{sense}$.

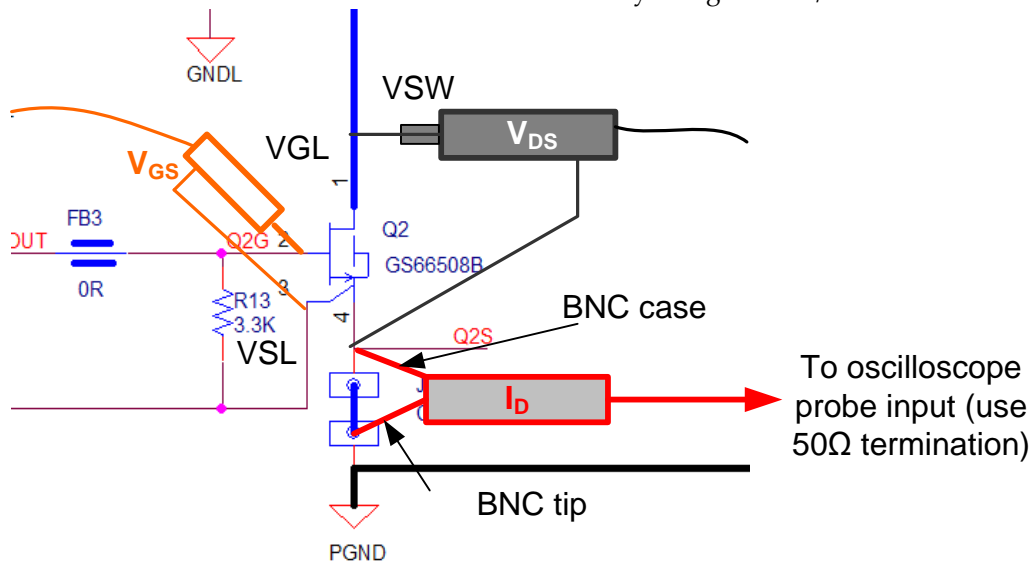


Figure 8 Recommended probe connection with current shunt

Thermal design:

1. GS66508B has a thermal pad at the bottom side for heat dissipation. The heat is transferred to the bottom side of PCB using thermal vias and copper plane.
2. A heatsink (35x35mm size) can be attached to the bottom side of board for optimum cooling. Thermal Interface Material (TIM) is needed to provide electrical insulation and conformance to

the PCB surface. The daughter board evaluation kit supplies with a sample 35x35mm fin heatsink (not installed), although other heatsinks can also be used to fit users' system design.

3. A thermal tape type TIM (Bergquist® Bond-Ply 100) is chosen for its easy assembly. The supplied heatsink has the thermal tape pre-applied so simply peel off the protective film and attach the heatsink to the back of board as marked in Figure 3.
4. Two optional mounting holes as shown in Figure 9 are provided for mounting customized heatsink using screws.
5. Using the supplied heatsink and TIM, the overall junction to ambient thermal resistance R_{thj-A} is $\sim 9^{\circ}\text{C}/\text{W}$ with 500LFM airflow.
6. Forced air cooling is recommended for power testing.

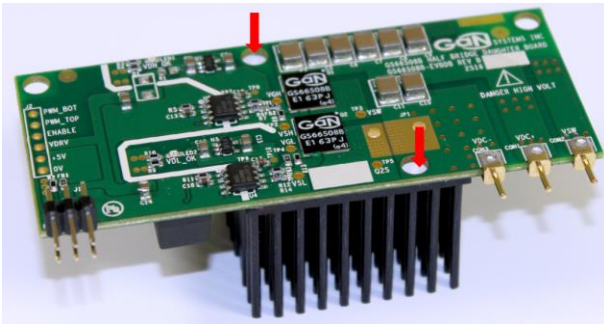


Figure 9 The daughter board with heatsink attached

CAUTION:

There is no on-board over-temperature protection. Device temperature must be closely monitored during the test. Never operate the board with device temperature exceeding T_{J_MAX} (150°C)

Using GS665XXX-EVBDB with universal mother board GS665MB-EVB

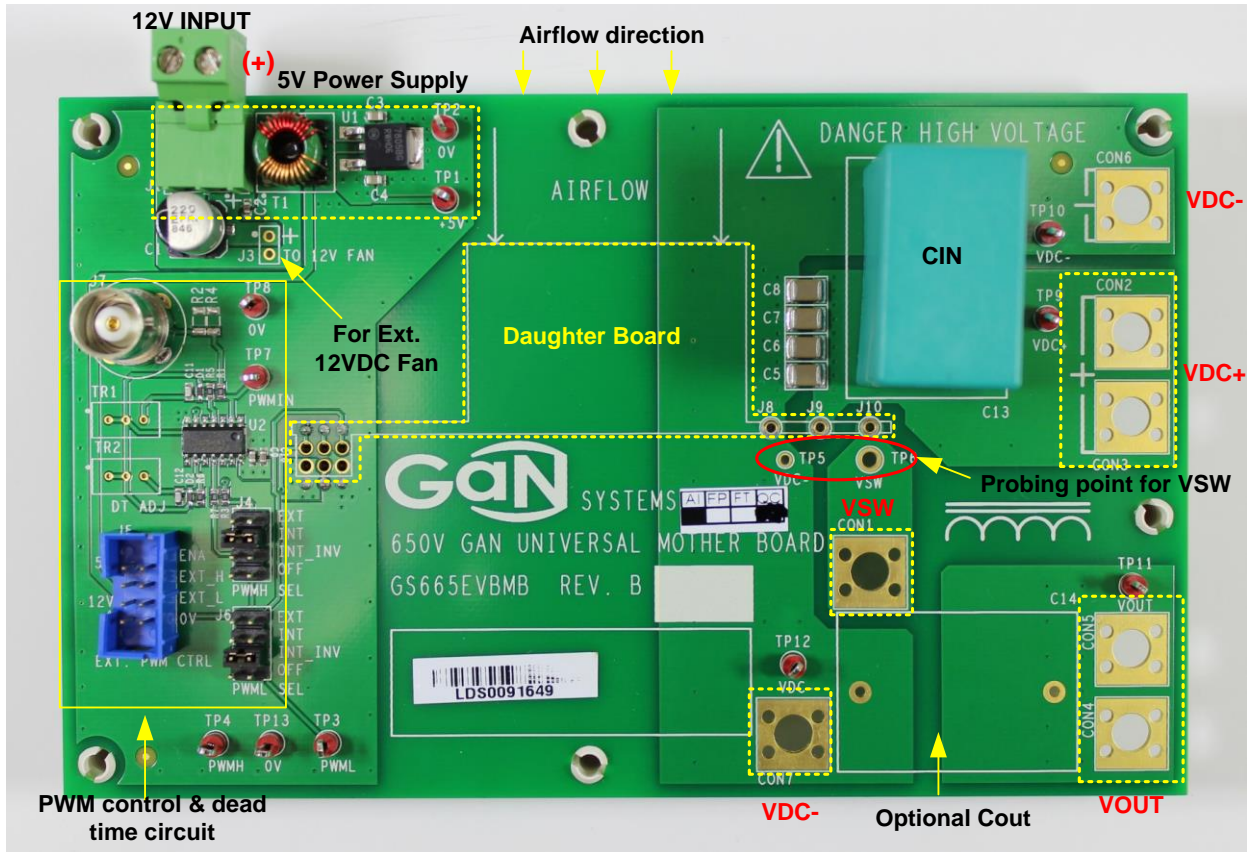


Figure 10 650V universal mother board GS665MB-EVB

GaN Systems provides a universal 650V mother board (ordering part number: GS665MB-EVB, sold separately) that can be used as the basic evaluation platform for all the daughter boards.

The universal 650V mother board evaluation kit includes following items:

1. Mother board GS665MB-EVB
2. 12VDC Fan

12V input:

The board can be powered by 9-12V on J1. On-board voltage regulator creates to 5V for daughter board and control logic circuits. J3 is used for external 12VDC fan.

PWM control circuit:

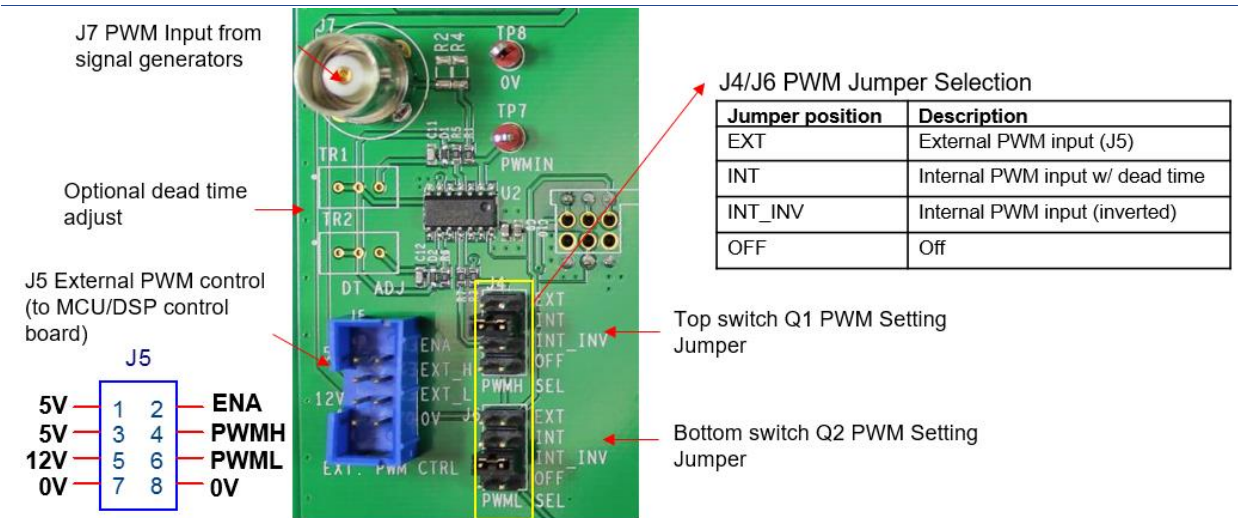


Figure 11 PWM control input and dead time circuit

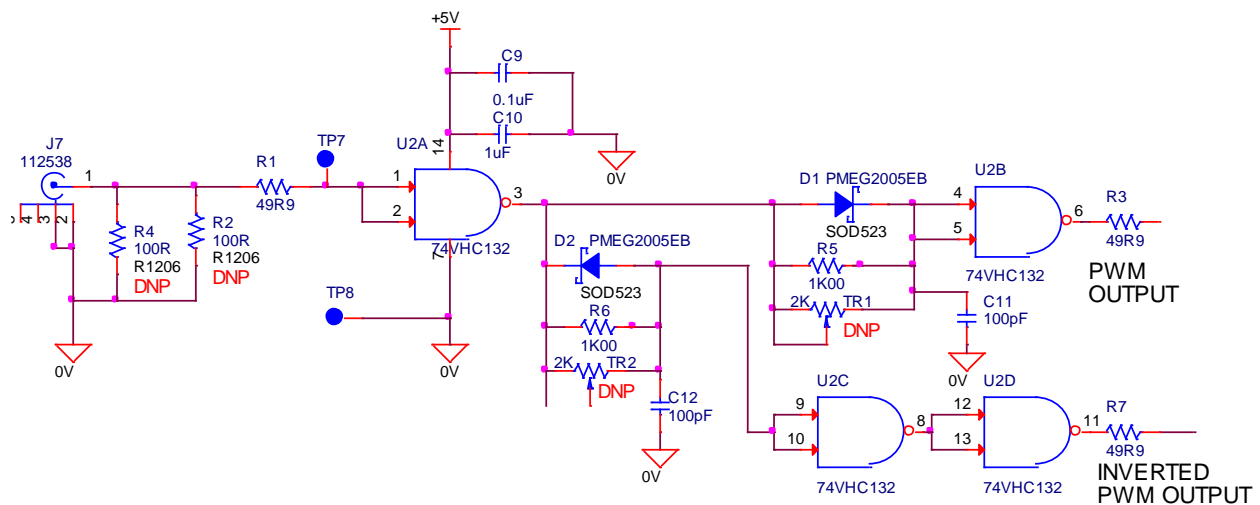


Figure 12 On board dead time generation circuit

The top and bottom switches PWM inputs can be individually controlled by two jumpers J4 and J6. Users can choose between a pair of complementary on-board internal PWM signals (non-inverted and inverted, controlled by J7 input) with dead time or external high/low side drive signals from J5 (users' own control board).

An on-board dead time generation circuit is included on the mother board. Dead time is controlled by two RC delay circuits, R6/C12 and R5/C11. The default dead time is set to about 100ns. Additionally two potentiometers locations are provided (TR1/TR2, not included) to allow fine adjustment of the dead time if needed.



WARNING!

ALWAYS double check the jumper setting and PWM gate drive signals before applying power. Incorrect PWM inputs or jumper settings may cause device failures

Test points:

Test points are designed in groups/pairs to facilitate probing:

Test points	Name	Description
TP1/TP2	+5V/0V	5V bias power
TP7/TP8	PWMIN/0V	PWM input signal from J7
TP4/TP3/TP13	PWMH/PWML/0V	High/low side gate signals to daughter board
TP9/TP10	VDC+/VDC-	DC bus voltage
TP11/TP12	VOUT/VDC-	Output voltage
TP6/TP5	VSW/VDC-	Switching node output voltage (for HV oscilloscope probe)

Power connections:

CON1-CON7 mounting pads are designed to be compatible with following mounting terminals:

- #10-32 Screw mount,
- Banana Jack PCB mount (Keystone P/N: 575-4), or
- PC Mount Screw Terminal (Keystone P/N: 8191)

Output passives (L and C14)

An external power inductor (not included) can be connected between VSW (CON1) and VOUT (CON4/5) or VDC+ (CON2/3) for double pulse test. Users can choose their inductor size to meet the test requirement. Generally it is recommended to use power inductor with low inter-winding capacitance to obtain best switching performance. For the double pulse testing we use 2x 60uH/40Amp inductor (CWS, P/N: HF467-600M-40AV) in series. C14 is designed to accommodate a film capacitor as output filter.

Double pulse test mode

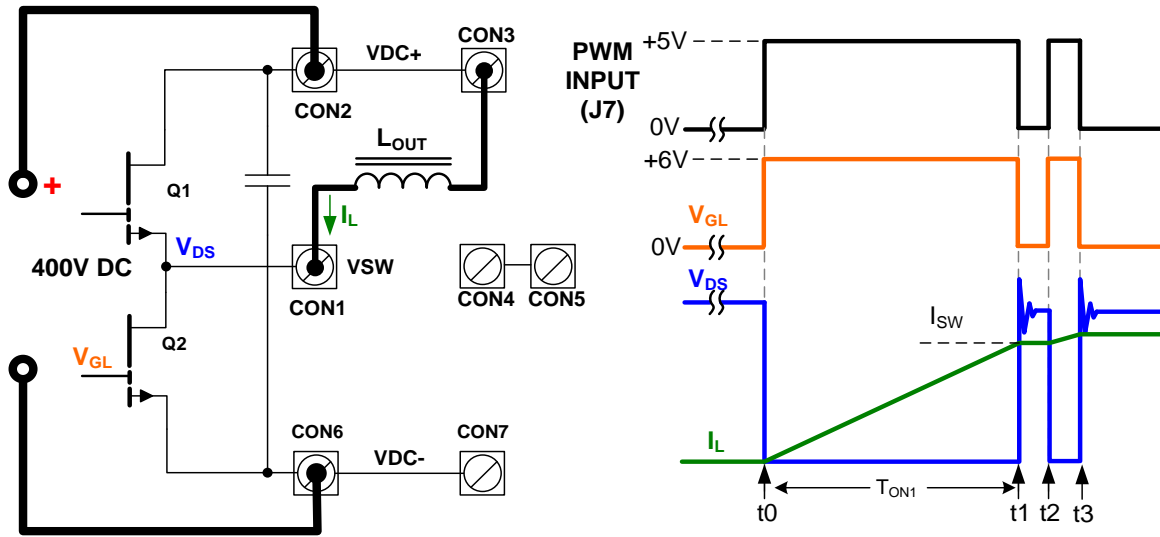


Figure 13 Double pulse test setup

Double pulse test allows easy evaluation of device switching performance at high voltage/current without the need of actually running at high power. It can also be used for switching loss (Eon/Eoff) measurement and other switching characterization parameter test.

The circuit configuration and operating principle can be found in Figure 13:

1. The output inductor is connected to the VDC+.
2. At t_0 when Q2 is switched on, the inductor current starts to ramp up until t_1 . The period of first pulse T_{ON1} defines the switching current $I_{SW} = (V_{DS} * T_{ON1}) / L$.
3. t_1 - t_2 is the free wheeling period when the inductor current I_L forces Q1 to conduct in reverse.
4. t_1 (turn-off) and t_2 (turn-on) are of interest for this test as they are the hard switching transients for the half bridge circuit when Q2 is under high switching stress.
5. The second pulse t_2 - t_3 is kept short to limit the peak inductor current at t_3 .

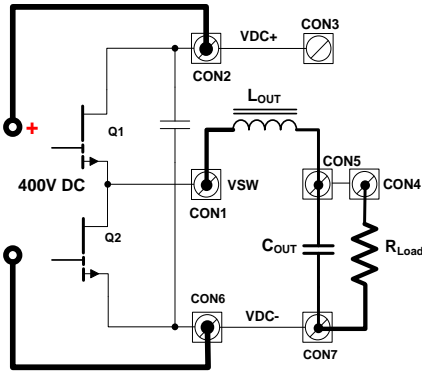
The double pulse signal can be generated using programmable signal generator or microcontroller/DSP board. As this test involves high switching stress and high current, it is recommended to set the double pulse test gate signal as single trigger mode or use long repetition period (for example >50-100ms) to void excess stress to the switches. Q1 can be kept off during the test or driven synchronously (J4 set to OFF or INT_INV) and Q2 is set to INT (or EXT position if PWM signal is from J5).



WARNING!

Limit the maximum switching test current to 30A and ensure maximum drain voltage including ringing is below 650V for pulse testing. Exceeding this limit may cause damage to the devices.

Buck/Standard half bridge mode



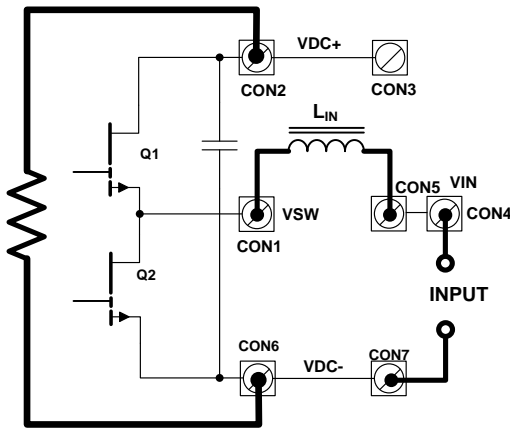
This is standard half bridge configuration that can be used in following circuits :

- Synchronous Buck DC/DC
- Single phase half bridge inverter
- ZVS half bridge LLC
- Phase leg for full bridge DC/DC or
- Phase leg for a 3-phase motor drive

Jumper setting:

- J4 (Q1): INT
- J6 (Q2): INT_INV

Boost mode



When the output becomes the input and the load is attached between VDC+ and VDC-, the board is converted into a boost mode circuit and can be used for:

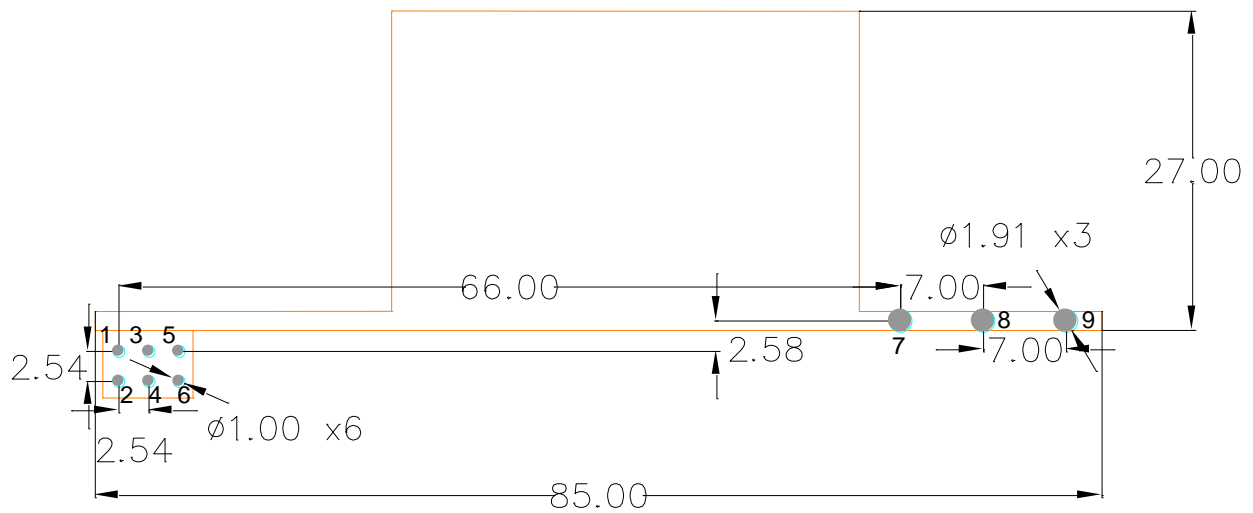
- Synchronous Boost DC/DC
- Totem pole bridgeless PFC

Jumper setting:

- J4 (Q1): INT_INV
- J6 (Q2): INT

Using GS665XXX-EVBDB in system:

The daughter board allows users to easily evaluate the GaN performance in their own systems. Refer to the footprint drawing of GS665XXX-EVBDB as shown below:



1. All units are in mm.
2. Pin 1-6: Dia. 1mm
3. Pin 7-9: 1.91mm (75mil) mounting hole for Mill-max Receptacle P/N: 0312-0-15-15-34-27-10-0.

Figure 14 Recommended footprint drawing of daughter board GS665XXX-EVBDB

Quick Start procedure – Double pulse test

Follow the instructions below to quickly get started with your evaluation of GaN E-HEMT. Equipment and components you will need:

- Four-channel oscilloscope with 500MHz bandwidth or higher
 - high bandwidth (500MHz or higher) passive probe
 - high bandwidth (500MHz) high voltage probe (>600V)
 - AC/DC current probe for inductor current measurement
 - 12V DC power supply
 - Signal generator capable of creating testing pulses
 - High voltage power supply (0-400VDC) with current limit.
 - External power inductor (recommend toroid inductor 50-200uH)
1. Check the JP1 on daughter board GS665XXX-EVBDB. Use a copper foil and solder to short JP1.
 2. Install GS665XXX-EVBDB on the mother board. Press all the way down until you feel a click. Connect probe between VGL and VSL for gate voltage measurement.
 3. Set up the mother board:
 - a. Connect 12VDC bias supply to J1.
 - b. Connect PWM input gate signal (0-5V) to J7. If it is generated from a signal generator ensure the output mode is high-Z mode.
 - c. Set J4 to OFF position and J7 to INT.
 - d. Set High voltage (HV) DC supply voltage to 0V and ensure the output is OFF. Connect HV supply to **CON2** and **CON6**.
 - e. Use HV probe between TP6 and TP5 for Vds measurement.
 - f. Connect external inductor between **CON1** and **CON3**. Use current probe to measure inductor current IL.
 4. Set up and check PWM gate signal:
 - a. Turn-on 12VDC power.
 - b. Check the 2 LEDs on the daughter board. They should be turned on indicating the isolated 9V is present.
 - c. Set up signal generator to create the waveforms as shown in Figure 13. Use equation $I_{sw} = (V_{DS} * T_{ON1}) / L$ to calculate the pulse width of the first pulse and ensure the I_{sw_max} is $\leq 30A$ at 400VDC.
 - d. Set the operation mode to either single trigger or Burst mode with repetition period of 100ms.
 - e. Turn on the PWM output and check on the oscilloscope to make sure the VGL waveform is present and matches the PWM input.
 5. Power-on:
 - a. Turn on the output of the HV supply. Start with low voltage and slowly ramp the voltage up until it reaches 400VDC. During the ramping period closely observe the the voltage and current waveforms on the oscilloscope.
 6. Power-off:
 - a. After the test is complete, slowly ramp down the HV supply voltage to 0V and turn off the output. Then turn off the 12V bias supply and signal generator output.

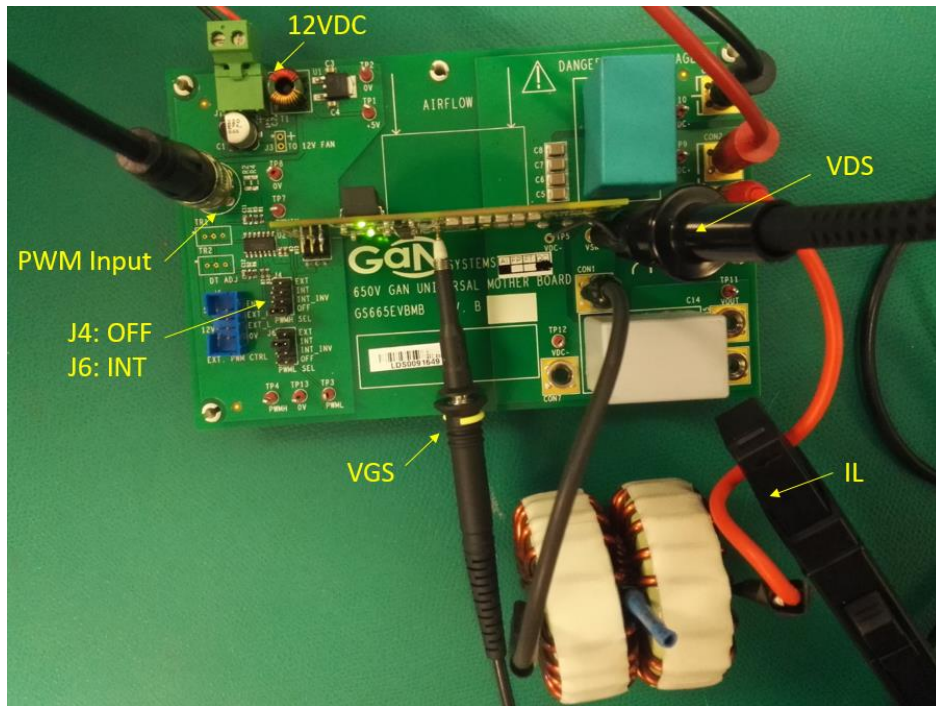


Figure 15 Double pulse test setup example (GS66508B-EVBDB)

Test results – GS66508B-EVBDB

Double Pulse test ($V_{DS}=400V$, $I_{MAX} = 30A$, $L=120\mu H$, $R_{G(ON)}=10\Omega$, $R_{G(OFF)}=1\Omega$):

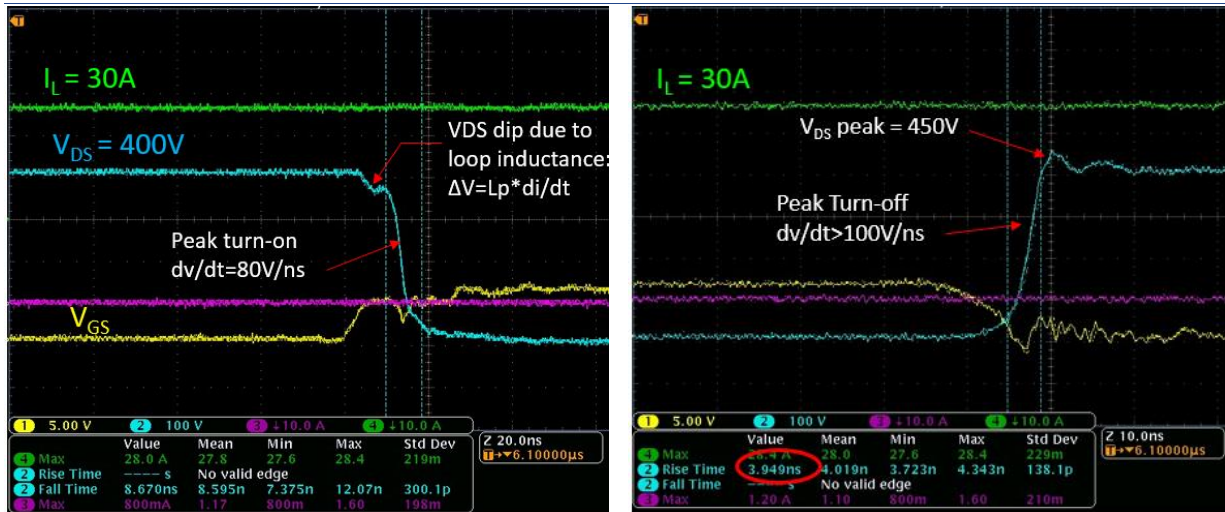


Figure 16 400V/30A double pulse test waveform

Figure 16 shows the hard switching on waveforms at 400V/30A. A V_{ds} dip can be seen due to the rising drain current (di/dt in the power loop $\Delta V=L_p \times di/dt$, where L_p is the total power loop inductance). After the drain current reaches the inductor current, the V_{ds} starts to fall. The V_{gs} undershoot spike is caused by the miller feedback via C_{gd} under negative dv/dt .

Due to the low gate charge and small $R_{G(OFF)}$, GaN E-HEMT gate has limited control on the turn-off dv/dt . Instead the V_{ds} rise time is determined by how fast the turn-off current charges switching node capacitance (C_{oss}).

The low C_{oss} of GaN E-HEMT and low parasitic inductance of GaNPX™ package together with optimized PCB layout, enables a fast and clean turn-off V_{ds} waveform with only 50V the turn-off V_{ds} overshoot at $dv/dt > 100V/ns$. The measured rise time is 3.9ns at 400V and 30A hard turn-off.



a) hard switching turn-on 400V/30A

b) hard switching turn-off 400V/30A

Figure 17 Double puls test switching transient waveforms

Switching Loss energy (Eon/Eoff) measurement

A T&M search coaxial current shunt (SDN-414-10, 0.1Ω) is installed for switching loss measurement as shown below.

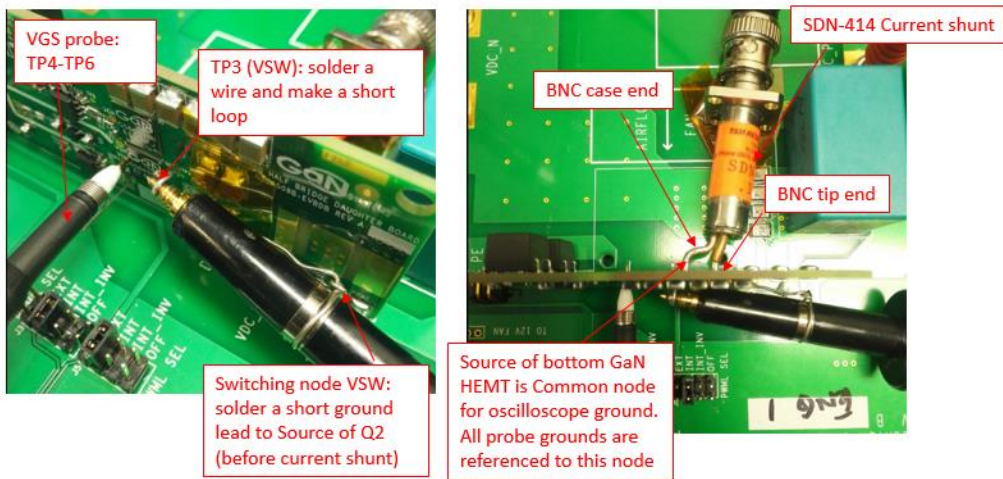


Figure 18 Eon/Eoff measurement probe connection with current shunt

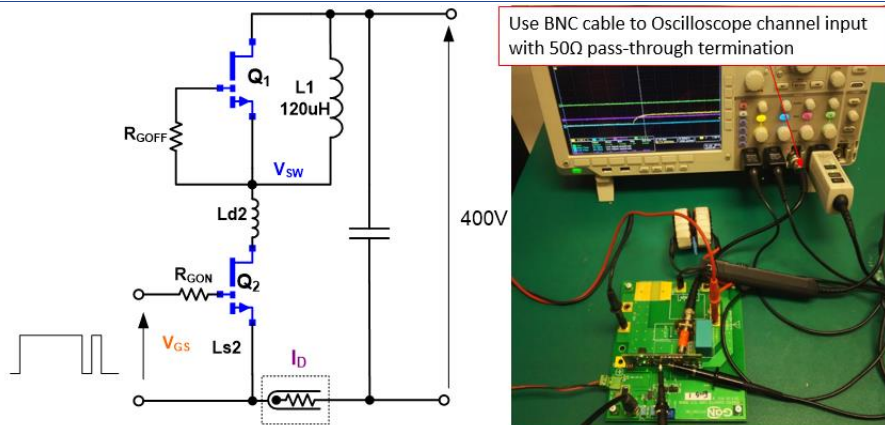


Figure 19 Eon/Eoff measurement and test bench setup

The switching energy can be calculated from the measured switching waveform $P_{sw} = V_{ds} \cdot I_d$. The integral of the P_{sw} during switching period is the measured switching loss. The channel deskewing is critical for measurement accuracy. It is recommended to manually deskew I_d against V_{ds} as shown in Figure 20. The drain current spike is caused by charging the high side switch C_{oss} (Q_{oss} loss).



Figure 20 Turn-on switching loss measurement ($E_{on}=113\mu J$, 400V/30A)

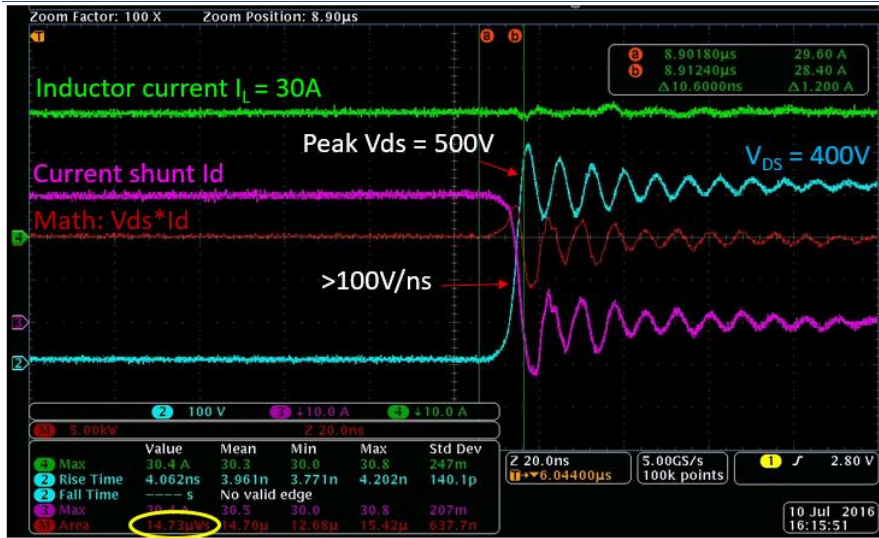


Figure 21 Turn-off switching loss measurement (E_{off}=15μJ, 400V/30A)

The switching loss measurements with drain current from 0 to 30A can be found in Figure 22. The turn-on loss dominates the overall hard switching loss. E_{on} at 0A is the Q_{oss} loss caused by the C_{oss} at high side switch.

The turn-off loss remain almost constant from 0A up to 20A about 8μJ. the measured E_{off} matches well with the E_{oss} @400V, which indicates that turn-off energy is dominated by E_{oss}, the energy required to charge C_{oss} from 0V to bus voltage. This energy is not part of loss at turn-off, but actually part of turn-on loss at next hard switching turn-on period. This means that with the fast turn-off speed the GaN E-HEMT can achieve near zero turn-off switching loss.

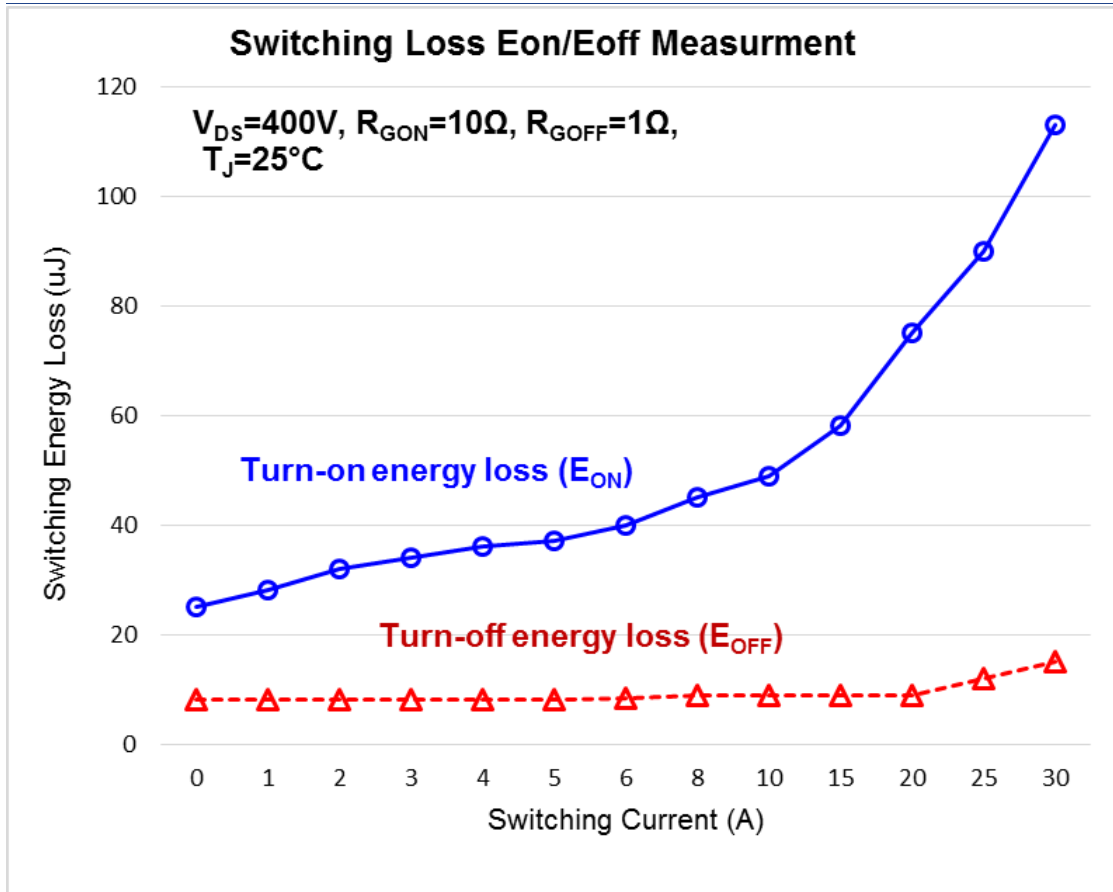


Figure 22 GS66508B Switching Loss Measurement ($V_{DS} = 400V$, $T_J=25^\circ C$)

Synchronous Buck Test (L=120uH, VIN=400V, VOUT=200V, D=50%, FSW=100 kHz, POUT =0-1.5kW)

The board is converted to a synchronous buck DC/DC converter and demonstrates efficiency 99% at 1.5kW. With forced air cooling, the peak device temperature T_{J_MAX} was measured at 80°C at 1kW output.

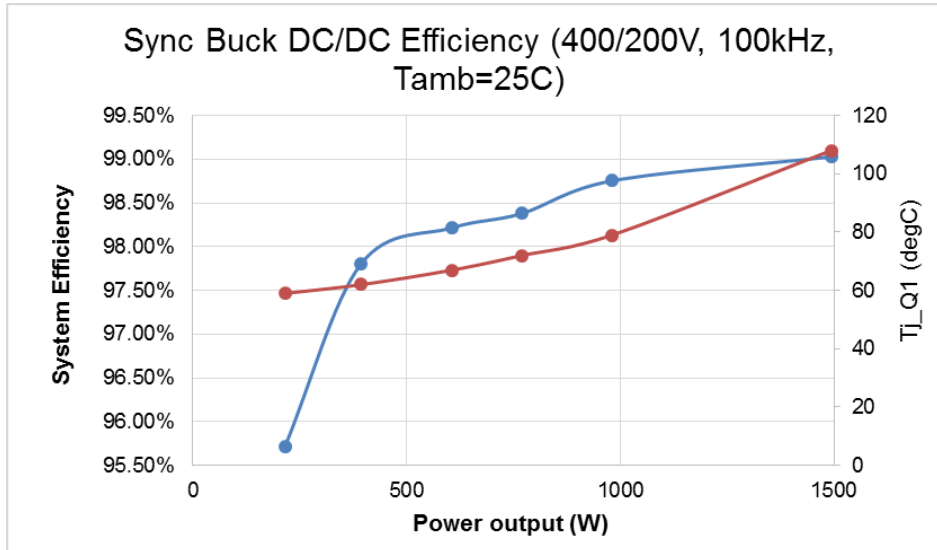


Figure 23 Synchronous Buck Efficiency and thermal measurement

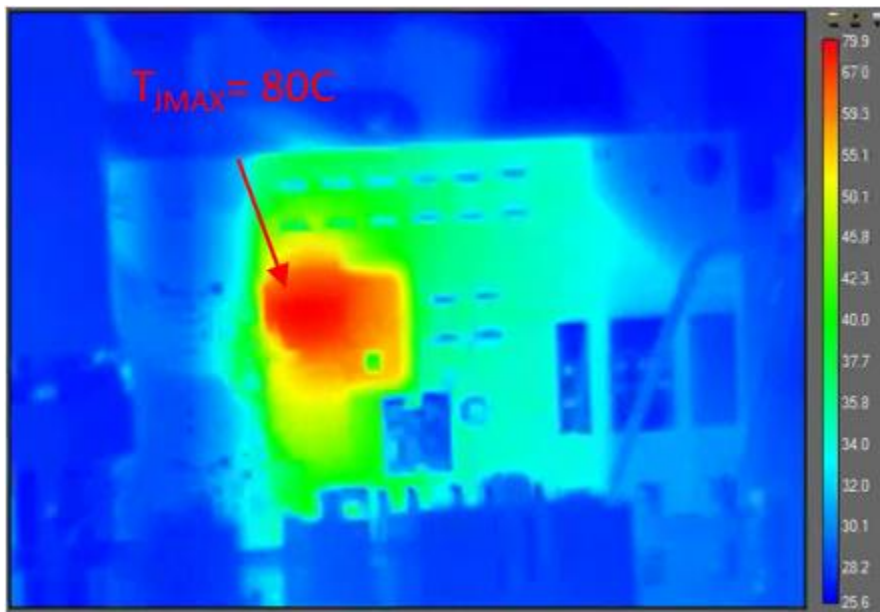
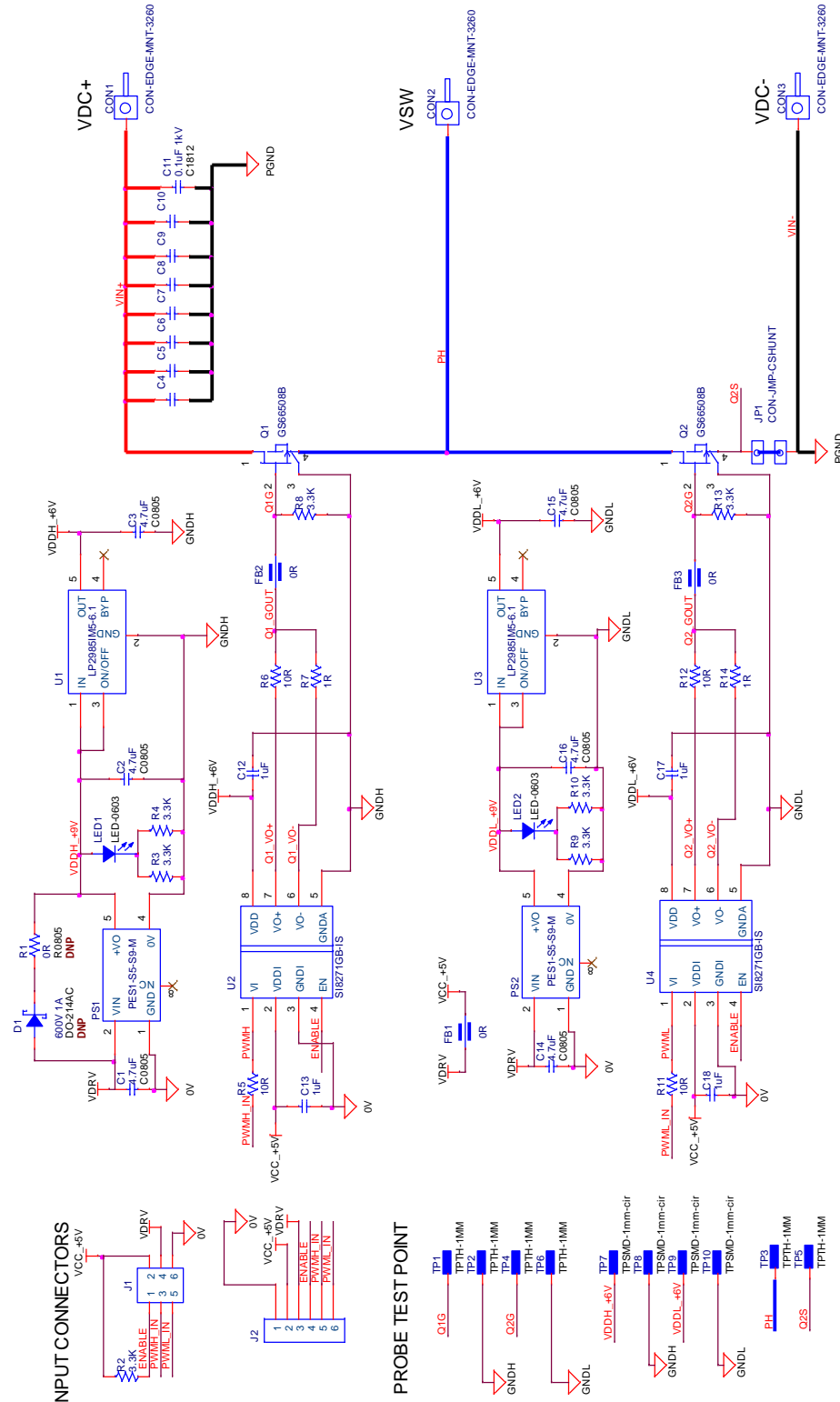


Figure 24 Thermal image (Pout=1kW)

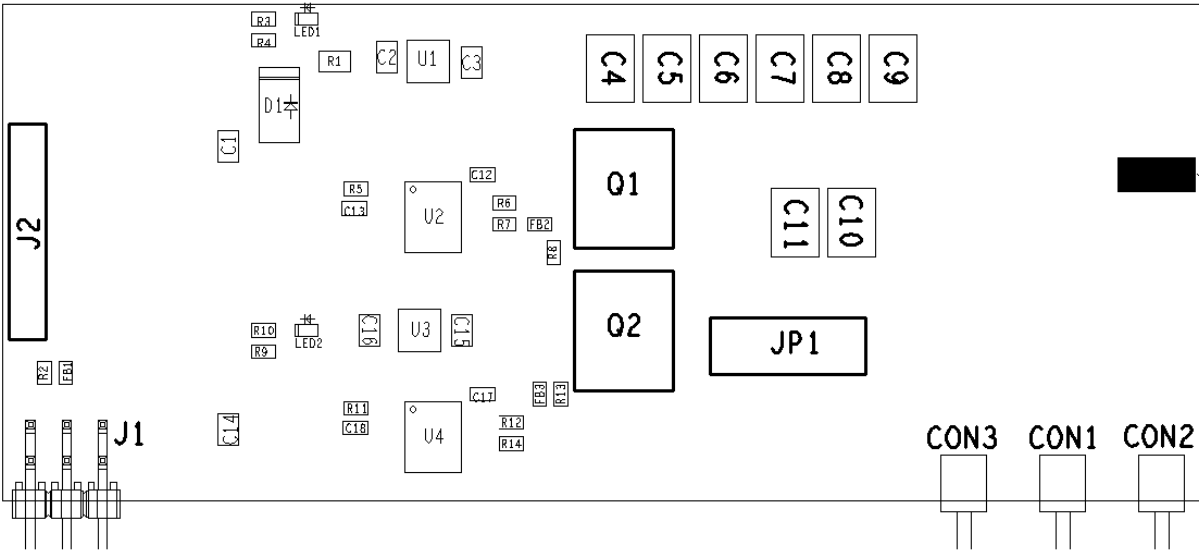
Appendix A - GS66508B-EVBDB

Circuit schematics

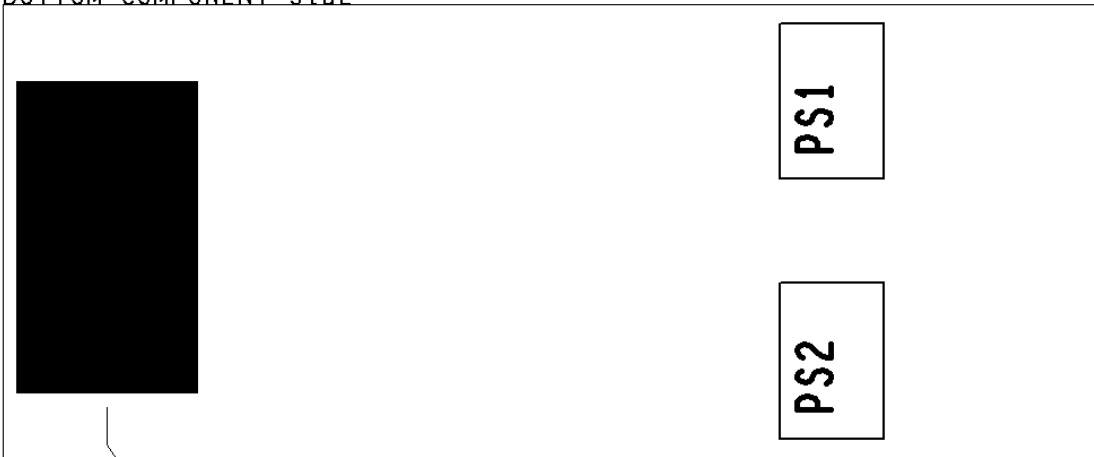


Assembly Drawing

TOP COMPONENT SIDE



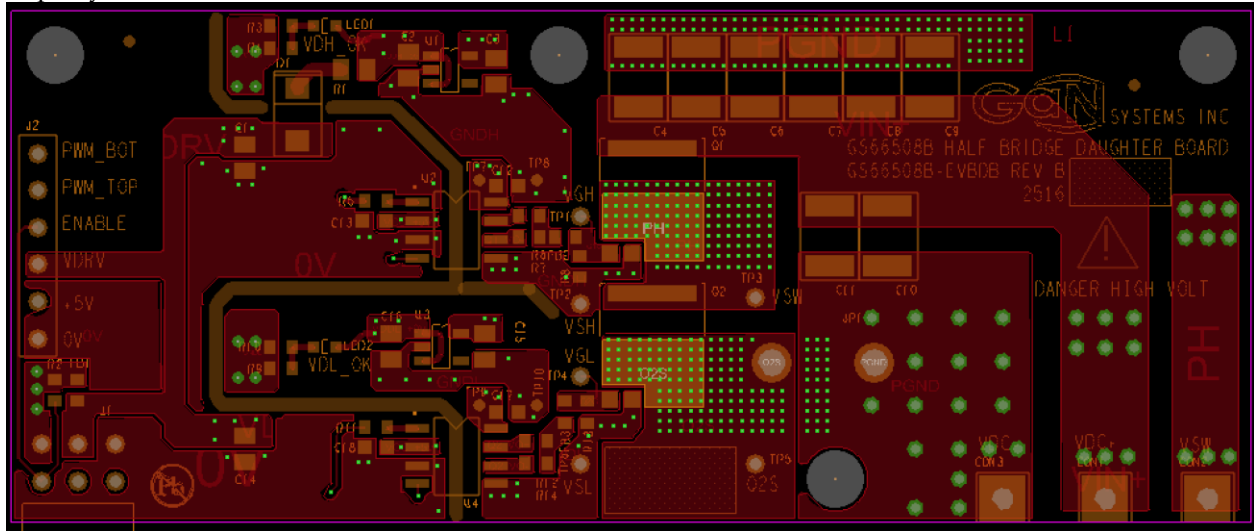
BOTTOM COMPONENT SIDE



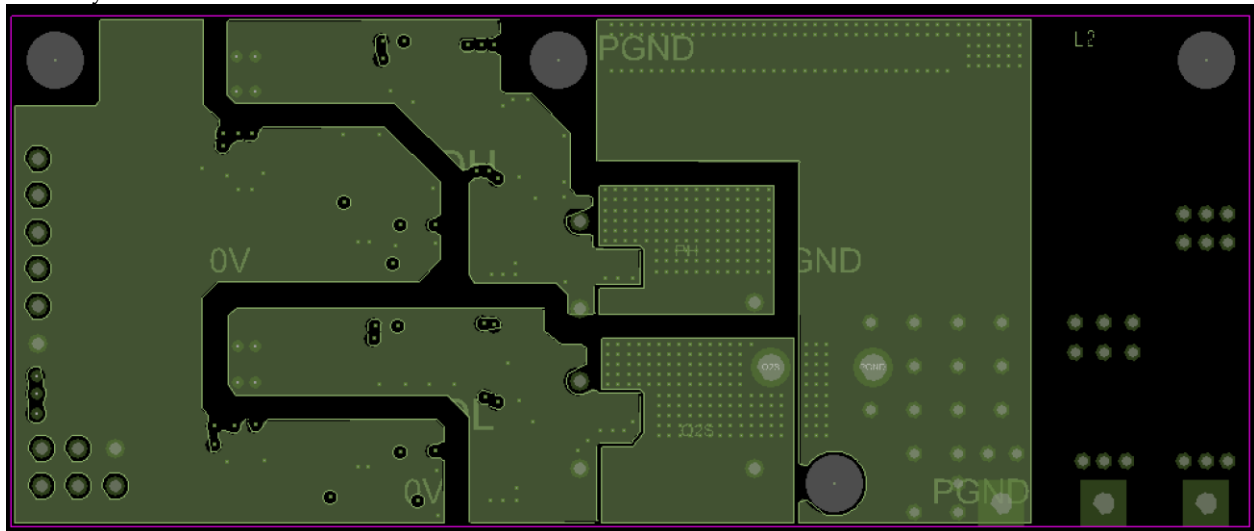
SUGGESTED LOCATION FOR S/N LABEL , INSTALL LABEL AFTER FINAL WASH

PCB layout

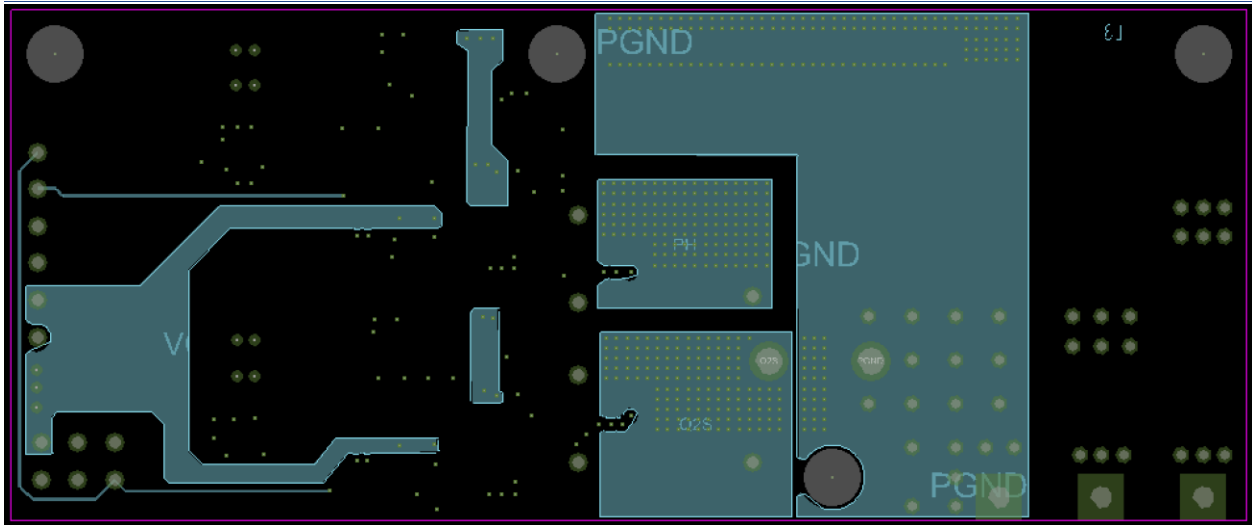
Top Layer



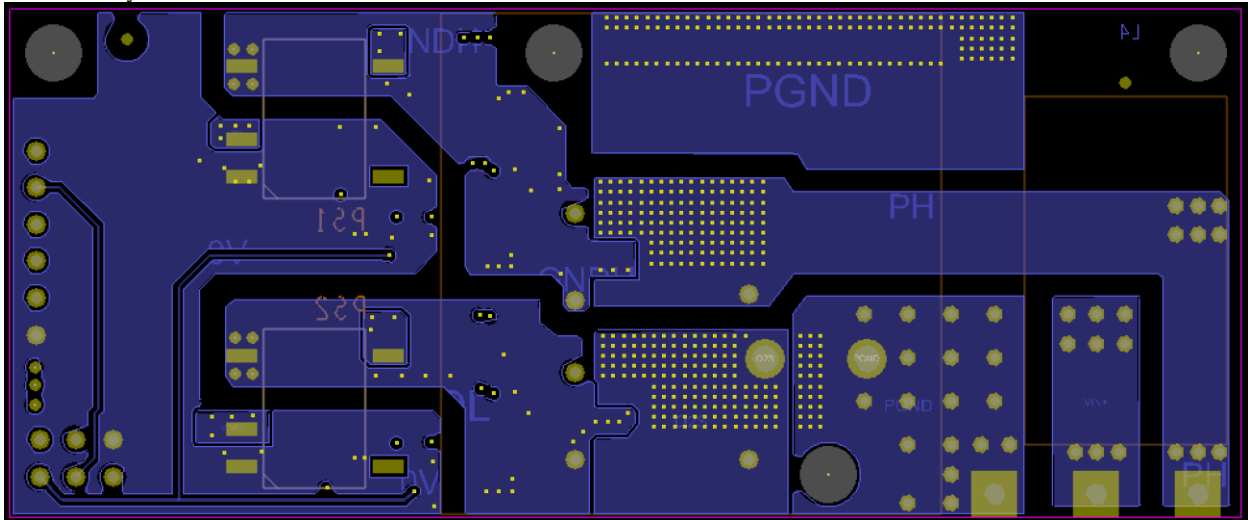
Mid Layer 1



Mid Layer 2



Bottom Layer

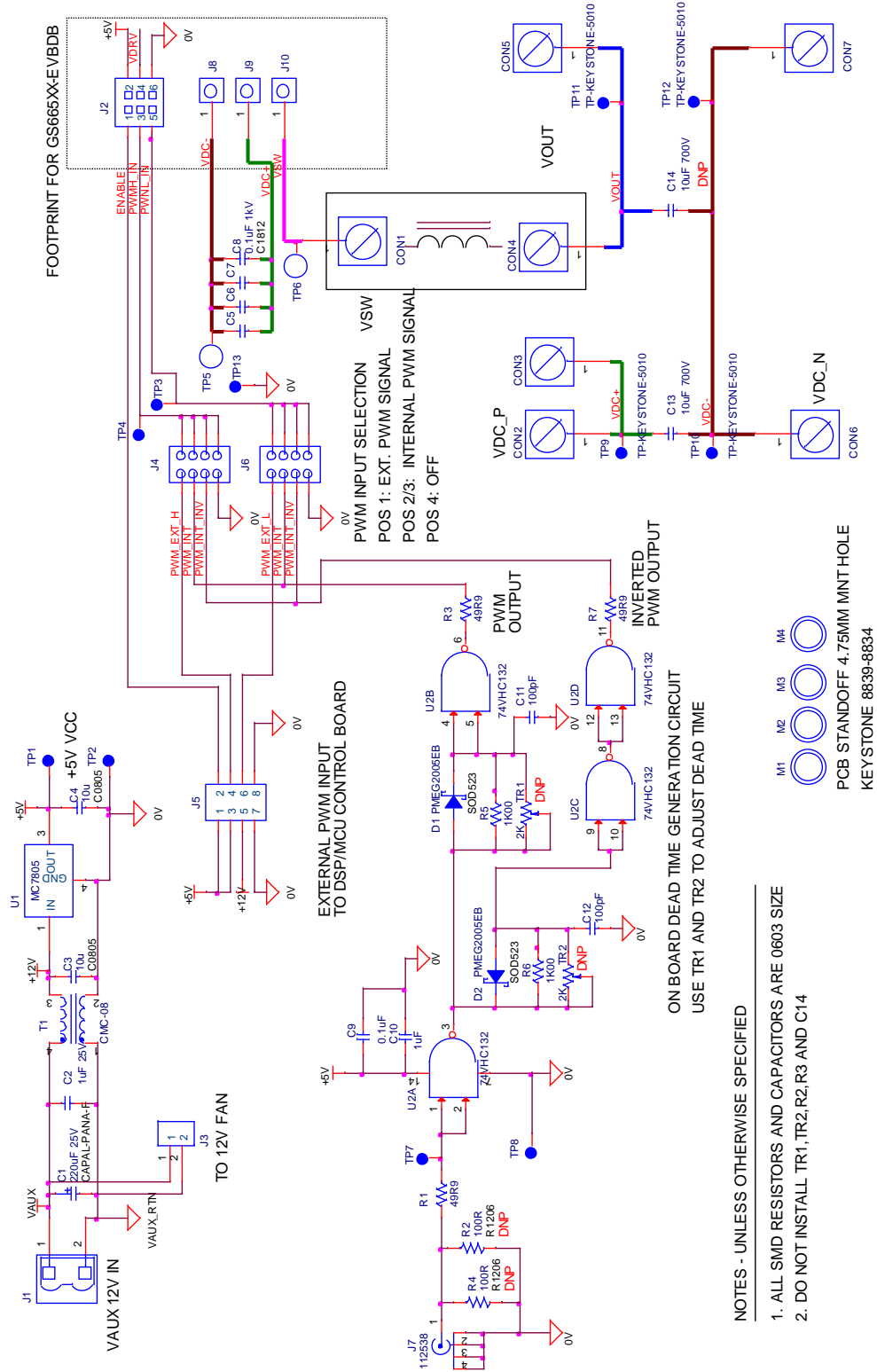


Bill of Materials

Quantity	Reference	Description	Value	Manufacturer	Part number	Assembly Note
GS66508B HALF BRIDGE DAUGHTER CARD 2016-06-10 BOARD NAME: GS66508B-EVBDB Revision: B1 Last Update: 20160624						
1	PCB	PCB bare 4-layer 2oz Cu.				
3	CON1,CON2,CON3	CONN PC PIN EDGE MNT	CON-EDGE-MNT-3266	MIL-Max	3620-2-32-15-00-00-08-0	mounting receptacle on mother board:0312-0-15-15-34-27-10-0
2	C1,C2,C3,C14,C15,C16	CAP, CER, 4.7UF, 25V, +/-10%, X7R, 0603	4.70F	TAYO YUDEN	TMK212AB7475KG-T	
3	C4,C5,C6,C7,C8,C9,C10,C11	CAP, CER, 0.1UF, 1KV, +/-10%, X7R, 1812	0.1uF 1KV	KEMET	C1812C104KDRAC7800	
4	C12,C13,C17,C18	CAP, CER, 1UF, 25V, +/-10%, X7R, 0603	1uF	TAYO YUDEN	TMK107B7105KA-T	
5	D1	DIODE ULTRAFast 600V 1A SMA	600V 1A	FAIRCHILD	ES1J	For bootstrap mode, DO NOT INSTALL
3	FB1,FB2,FB3	0R JUMPER 0603	0R	generic 1% 100ppm 0603		
7	1JP1	CURRENT SHUNT JUMPER	CON-JMP-C-SHUNT			For current measurement, footprint compatible with T&M SDN-414-010 current shunt. Use wide copper foil to short the connection if not used for better
8	1J1	CONN 3PIN DUAL ROW, 0.1" PITCH, R/A	CON-HDR-2X3	HARWIN INC.	M20-9950345	
9	1J2		CON-6POS			DO NOT INSTALL
2	LED1,LED2	LED, GREEN, SMD 0603	LED-SMD-0603	liteon	11st-c191kgkt	
2	PS1,PS2	ISO. DC/DC 5-9V, 1W	PES1-S5-S9-M	cui	PES1-S5-S9-M	
2	Q1,Q2	GaN E-HEMT 650V/30A	GS66508B	GaN Systems	GS66508B	
1	R1	RES 0 R, 1%, 0805	0R			For bootstrap mode, DO NOT INSTALL
7	R2,R3,R4,R8,R9,R10,R13	RES, 3.3K, 1%, 1/10W, 0603	3.3K	generic 1% 100ppm 0603		
4	R5,R6,R11,R12	RES, 10R, 1%, 1/10W, 0603	10R	generic 1% 100ppm 0603		
2	R7,R14	RES, 1R, 1%, 1/10W, 0603	1R	generic 1% 100ppm 0603		
6	TP1,TP2,TP3,TP4,TP5,TP6	Probe test point	CON-TP-1POS			DO NOT INSTALL
4	TP7,TP8,TP9,TP10	Probe test point	CON-TP-1POS			DO NOT INSTALL
2	U1, U3	REG LDO 6V, 100mA, STO23-5	LP2985IM5-6.1	TEXAS INSTRUMENTS	LP2985IM5-6.1/NOPB	
2	U2, U4	IC ISO GATE DRIVER 2.5KV HIGH CMTI	S18271GB-IS	SILICON LABS	S18271GB-IS	
Off the board components:						
1		heatsink, 35x35mmx25.4mm, black anodized		Cool Innovation	3-141410UBLAN	DO NOT install on the PCB assembly, supply loose with pre-applied Thermal sheet (item #22)
1		Thermal sheet cut to 35x35mm square		bergquist	BOND PLY 100	Bondply 100 thermal adhesive tape cut to 35x35mm and apply to heatsink surface (item #21)

Appendix B - GS665MB-EVB

Circuit schematics



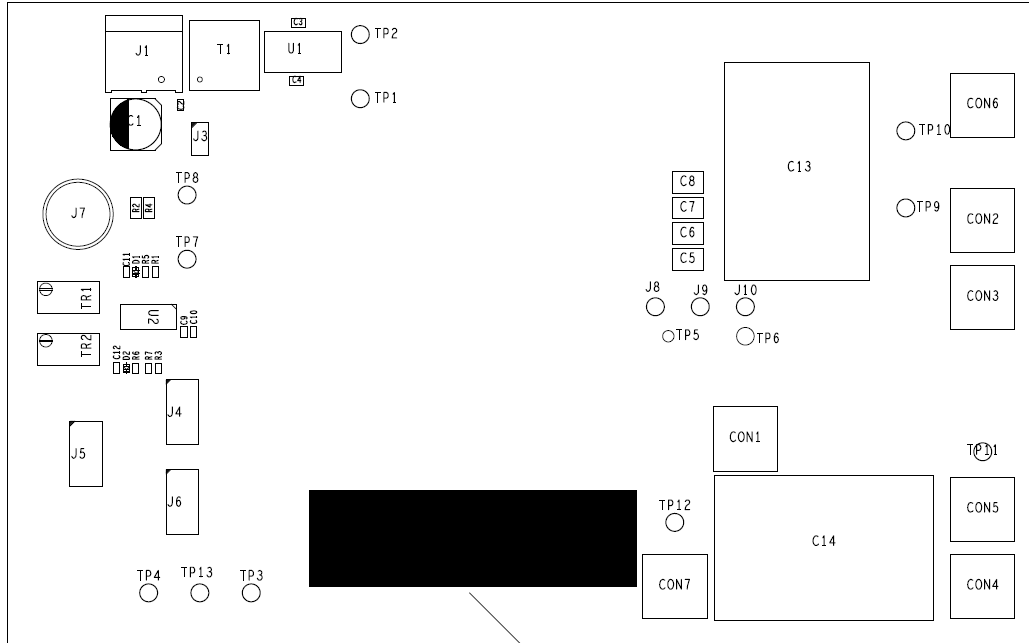
NOTES - UNLESS OTHERWISE SPECIFIED

1. ALL SMD RESISTORS AND CAPACITORS ARE 0603 SIZE
2. DO NOT INSTALL TR1, TR2, R3 AND C14

Assembly drawing

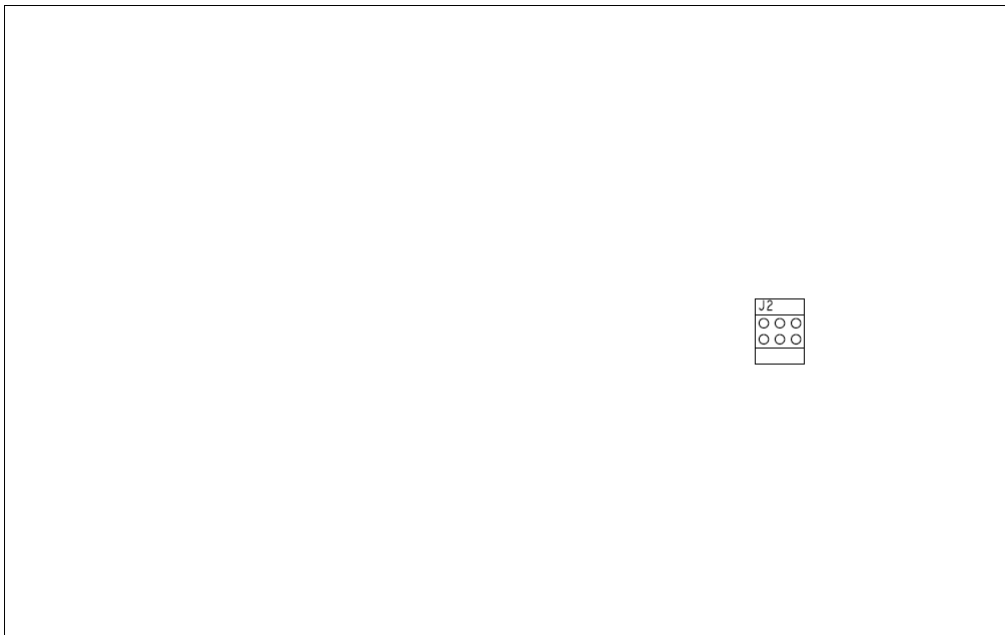
Assembly Top

TOP COMPONENT SIDE



SUGGESTED LOCATION FOR S/N LABEL

Assembly Bottom



Bill of Materials

Quantity	Reference	Description	Value	Manufacturer	Part number	Assembly Note
1	PCB	PCB bare 2-layer 2oz Cu.				
1	CON1,CON2,CON3,CON4,C ON5,CON6,CON7	TERMINAL SCREW VERTICAL PC MNT	CON-10-32-SCRWMNT	KEYSTONE	8191	DO NOT INSTALL
2	1 C1	CAP ALUM 220UF 20% 25V SMD	220uF 25V	Panasonic	EEE-FK1E221P	
3	1 C2,C10	GENERIC 1UF/25V, 10% X7R SMD 0603	1uF	TAIYO YUDEN	TMK107B7105KA-T	
4	2 C3,C4	GENERIC 10UF/25V, 10% SMD 0805	10uF	TAIYO YUDEN	TMK212BBJ106KG-T	
5	4 C5,C6,C7,C8	GENERIC 0.1UF/1000V, SMD 1812	0.1uF 1kV	KEMET	C1812C104KDRAC7800	
6	1 C9	GENERIC 0.1UF/25V, 10% X7R SMD 0603	0.1uF	TAIYO YUDEN	TMJ107BB7104KAHT	
7	2 C11,C12	GENERIC 100PF/25V, 5% NPO SMD 0603	100pF	KEMET	C0603C101J3GACTU	
8	1 C13,C14	CAP FILM 10UF/600VDC 5%, 27.5MM LEAD SPACING	10uF 700V	KEMET	C4AEHBU5100A11J	DO NOT INSTALL C14
9	2 D1,D2	DIODE SCHOTTKY 20V 500MA SOD523	PMEG2005EB	NXP	PMEG2005EB,115	
10	1 J1	TERM BLOCK HDR 2POS R/A 5.08MM	CON-TERM-BLK-2POS-RA	TE CONNECTIVITY	796638-2	
11	1 J1-PLUG	TERM BLOCK BLUG 2POS 5.08MM	CON-CONNECTIVITY	TE CONNECTIVITY	796634-2	
12	1 J2	CONN RCPT 6POS .100 DBL STR PCB	CON-RCPT-2X3-BOT	HARWIN	M20-7850342	MOUNT FROM BOTTOM SIDE CONNECTOR FOR 12V FAN, DO NOT INSTALL
13	1 J3		CON-2POS			
14	2 J4,J6	CONN HEADER 8POS DUAL VERT PCB	CON-JMP-4POS	HARWIN	M20-9980445	
15	1 J5	CONN 8-POS, DUAL ROW 2.54MM	CON-HDR-4X2	AMPHENOL	75869-132LF	
16	1 J7	CONN BNC JACK STR 50 OHM PCB	112538	AMPHENOL	112538	
17	3 J8,J9,J10	CONN RECEPT PIN .032-.046" .075"	CON-RCPT-EDGE MNT	MILLMAX	0312-0-15-15-34-27-10-0	MATING SOCKET FOR MILLMAX EDGE MNT PIN
18	3 R1,R3,R7	generic 1% smd 0603	49R9	VISHAY DALE	CRCW060349R9FKEA	
19	2 R2,R4	generic 1% smd 1206	100R			DO NOT INSTALL
20	2 R5,R6	generic 1% smd 0603	1K00	VISHAY DALE	CRCW06031K00FKEA	
21	TP1,TP2,TP3,TP4,TP7,TP8, TP9,TP10,TP11,TP12,TP13	TEST POINT PCB	TP-KEYSTONE-5010	KEYSTONE	5010	DO NOT INSTALL
22	2 TR1,TR2		2K	RECOM	CMC-08	
23	1 T1	COMM MODE CHOKE 5.2A TH	CMC-08			
24	1 U1	IC REG LDO 5V 1A DPAK	MC7805	ON SEMI	MC7805BDTRKG	
25	1 U2	1 IC GATE NAND 4CH 2-IMP 14-SOIC	74VHC132	FAIRCHILD	74VHC132MX	
Off the board components:						
26	6 M1,M2,M3,M4,M5,M6	PCB STANDOFF NYLON STACKABLE 4.75M	MECH-STD OFF-KEYSTONE-8	KEYSTONE	8833	PCB SPACER, INSTALL FROM BOTTOM SIDE
27	1 FAN	FAN AXIAL 38X20MM 12VDC WIRE		SUNON FANS	PMD1238PKB1-A.(2).GN	SUPPLY LOOSE, DO NOT INSTALL ON THE ASSEMBLY INSTALL ON J4 "INT" POSITION AND J6 "INT_INV" POSITION
28	2 JUMPER	JUMPER SHUNT GENERIC		TE CONNECTIVITY	382811-8	

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